

1. A structure for use in a semiconductor package, said structure comprising:

a first adhesive material provided between a die and a circuit board, said first adhesive material in parallel to a length of a wirebond slot in said circuit board, said first adhesive material residing on a first side of said wirebond slot;

a second adhesive material provided between said die and said circuit board, said second adhesive material in parallel to said length of said wirebond slot in said circuit board; said second adhesive material residing on a second side of said wirebond slot; and

a third material provided on said circuit board and extending between said first and second materials to form a diversion dam for an encapsulation material.

2. The structure of claim 1, where said first material is an adhesive tape.

3. The structure of claim 2, where said adhesive tape is a double sided adhesive tape.

4. The structure of claim 1, where said second material is an adhesive tape.

5. The structure of claim 4, where said adhesive tape is a double sided adhesive tape.

6. The structure of claim 1, where said third material is an adhesive tape.

7. The structure of claim 6, where said adhesive tape is a single sided adhesive tape.

5 8. The structure of claim 1, wherein said third material is a thin layer of material applied to one or both of said die and said circuit board, at a location adapted to face an inlet for an encapsulation compound.

9. The structure of claim 1, wherein said third material resides on said die.

10 10. The structure of claim 1, wherein said third material resides on said circuit board.

11. The structure of claim 1, wherein said die is a memory die.

12. A processor system comprising:

a memory; and

15 a processor coupled to said memory, at least one of said processor and said memory being in the form of a die which is coupled to a circuit board by an adhesive system, said adhesive system comprising:

a first adhesive material provided between said die and said circuit board, said first adhesive material being in parallel to a length of a

first side of said wirebond slot;

a second adhesive material provided between said die and said circuit board, said second adhesive material being in parallel to said length of said wirebond slot in said circuit board; said second adhesive material residing on a second side of said wirebond slot; and

a third material provided on said circuit board and extending between said first and second materials to form a diversion dam for an encapsulation material.

13. The system of claim 12, where said first material is an adhesive tape.

14. The system of claim 13, where said adhesive tape is a double sided adhesive tape.

15. The system of claim 12, where said second material is an adhesive tape.

16. The system of claim 15, where said adhesive tape is a double sided adhesive tape.

17. The system of claim 12, where said third material is an adhesive tape.

18. The system of claim 17, where said adhesive tape is a single sided adhesive tape.

19. The system of claim 12, wherein said third material is a thin layer of material applied to one or both of said die and said circuit board at a location adapted to face an inlet for an encapsulation compound.

20. The system of claim 12, wherein said third material resides on said die.

21. The system of claim 12, wherein said third material resides on said circuit board.

22. The system of claim 12, wherein said die is a memory die.

23. A die mounting structure comprising:

a die;

a circuit board containing a wirebond slot;

a first piece of double side adhesive tape secured between said die and said circuit board, said first piece of tape being parallel to a length of said wirebond slot, said first piece of tape residing on a first side of said wirebond slot;

a second piece of double side adhesive tape secured between said die and said circuit board, said second piece of tape being parallel to said length of said wirebond slot in said circuit board; said second piece of tape residing on a second of said wirebond slot; and

a third piece of tape perpendicular to said first and second pieces of doubled sided tape, said third piece of tape contacting said first and second pieces of doubled sided tape to form an encapsulated diversion dam.

5 24. The structure of claim 23, where said third piece of tape is a single sided adhesive tape.

 25. The structure of claim 23, wherein said third piece of tape is provided at a location adapted to face an inlet for an encapsulation compound.

10 26. The structure of claim 23, wherein said third piece of tape resides on said die.

 27. The structure of claim 23, wherein said third piece of tape resides on said circuit board.

 28. The structure of claim 23, wherein said die includes a memory device.

15 29. The structure of claim 23, wherein said die includes a processor.

 30. A die mounting structure comprising:

 a die;

 a circuit board containing a wirebond slot;

a first piece of double side adhesive tape secured between said die and said circuit board, said first piece of tape being parallel to a length of said wirebond slot, said first piece of tape residing on a first side of said wirebond slot;

5 a second piece of double side adhesive tape secured between said die and said circuit board, said second piece of tape being parallel to said length of said wirebond slot in said circuit board; said second piece of tape residing on a second of said wirebond slot; and

10 a thin layer of material provided between said first and second pieces of doubled sided adhesive tape to form an encapsulation diversion dam.

31. The structure of claim 30, where said thin layer of material is at a location adapted to face an inlet for an encapsulation compound.

15 32. The structure of claim 31, wherein said thin layer of material resides on said die.

33. The structure of claim 31, wherein said thin layer of material resides on said circuit board.

34. The structure of claim 31, wherein said die includes a memory device.

20 35. The structure of claim 31, wherein said die includes a processor.

36. A method of encapsulating a semiconductor package, said method comprising:

securing a first adhesive material between a die and a circuit board, said first adhesive material extending in parallel to a length of a wirebond slot in said circuit board, said first adhesive material residing on a first side of said wirebond slot;

securing a second adhesive material between said die and said circuit board, said first adhesive material extending in parallel to said length of said wirebond slot in said circuit board, said first adhesive material residing on a second side of said wirebond slot;

securing a third material between said die and said circuit board and extending between said first and second adhesive materials; and

injecting a compound into a gate, said compound being directed by said third material to fill said wirebond slot last.

37. The method of claim 32 wherein said step of securing said third material comprises securing said third piece of tape on said die.

38. The method of claim 32 wherein said step of securing said third material comprises securing said third piece of tape on said circuit board.

39. The method of claim 32, wherein said step of securing said third material comprises applying a thin layer of material on said die, said thin

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 contacting said first and
 method of claim 32,
 comprises applying a thin
 layer of material contact
 a diversion dam.

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Year	1960	1961	1962	1963	1964	1965	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1960	1961	1962	1963	1964	1965	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	